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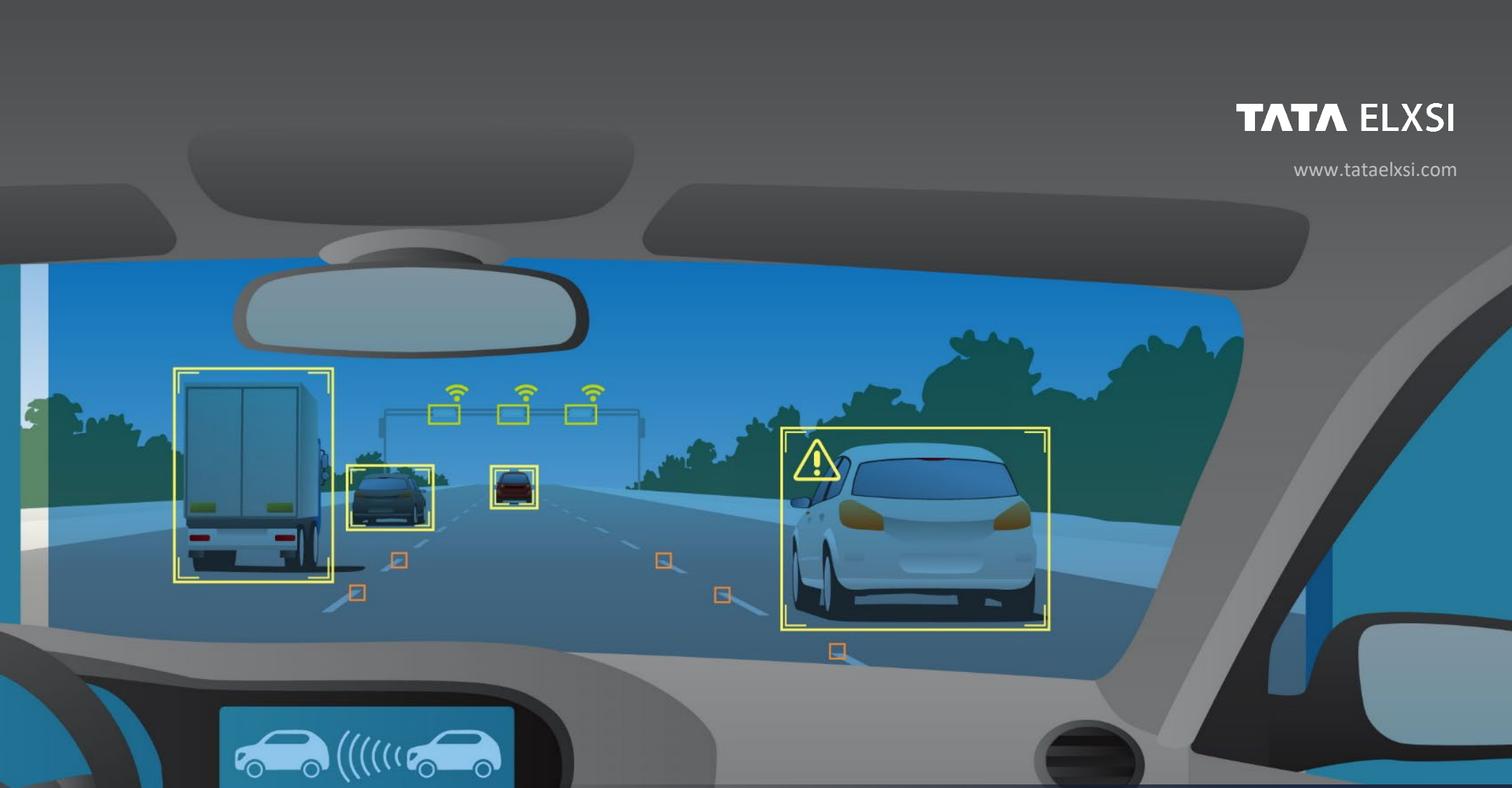


FPGA

Based ADAS Solution

TATA ELXSI

CASE STUDY

LOW LATENCY HIGH PERFORMANCE ADAS SOLUTION

Development of ADAS solution on FPGA for stereo disparity calculation using SGBM

Scope

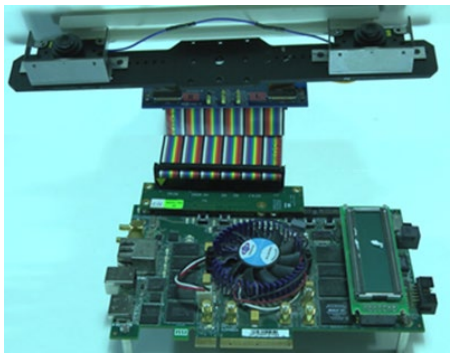
- Specification to complete product solution
- Object detection, Pedestrian detection, FCW
- Support for ICA, Auto Exposure Correction, Post processing filter to remove bad match

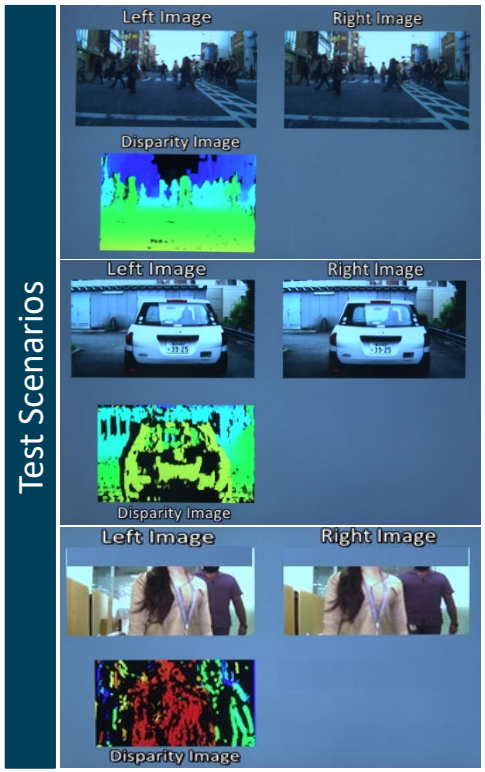
Challenges

- Optimum HW and SW partitioning by using internal process and domain expertise.
- Achieving real-time performance – sub-frame latency
  - Detecting depth using stereo camera
- Cost and power competitive with GPU based solutions
- Low cost FPGA device

Tools and Technologies

- Altera quarters tool, Processor IDE
- Altera Cyclone V device





Performance	Market	Business Benefit	Delivery Model	What's Next
Improvement from ~200ms/frame @30 fps to 35ms	Automotive	Cost effective solution on par with GPU	Fixed bid	Productization