DO254 DAL A FPGA Verification & Validation

Aerospace Tier 1, Germany

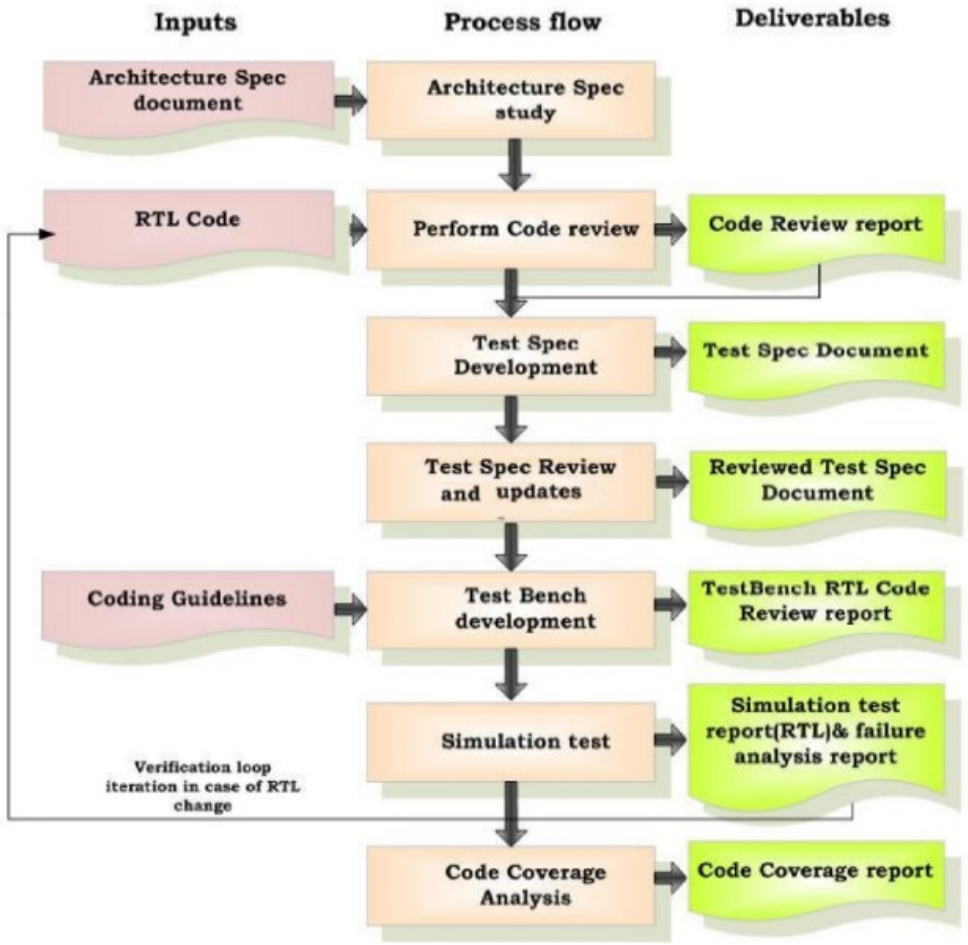
Summary

- Tata Elxsi scope is to carry out independent Verification & Validation of the RTL for DO254 Level A compliance in both at module level and FPGA level
- System is a dual redundant one, with features for detecting faults and selection of outputs.
- Load Master Work Station is located inside the cargo bay of an A400M
- Based on PowerPC CPU running at max 800 MHz, with three processor in lock-step mode

Challenges

- DO-254 based Verification of :
- Interfaces: CAN, AFDX, RS232, I2C and Wishbone
- Memories:
- Triple redundant Flash with two-out-of three voting
- RAM with ECC
- Controlling Logic for the interfaces and serial links implemented in Actel FPGA

Process Flow



DO254 DAL A FPGA Verification & Validation (contd)

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Scope

Module Level V&V

- Number of modules: 30
  - UART, I/O, voter, bus interface , DDR Controller , CAN controller, FSM
- Perform code reviews of VHDL source code
- Generate Test Specifications for 100% coverage
- Develop test cases, test benches
- Test case/bench reviews
- Simulation runs on Modelsim
- Code coverage analysis, Failure analysis
- Establish traceability to specifications

FPGA Level V&V

- Number of FPGAs: 6
  - Test specifications provided
- Perform code reviews of VHDL source code
- Develop test cases, test benches
- Test case/bench reviews
- Simulations
  - Functional
  - Post –layout (Min & Max timings)
- Failure analysis
- Establish traceability to specifications